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Date: 4/21/04 Deborah L. Corpus

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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re patent application of: | |
| Applicant(s): Bharath Rangarajan, *et al.* | Examiner: Binh X. Tran |
| Serial No: 09/845,454 | Art Unit: 1765 |
| Filing Date: April 30, 2001 | |

Title: SYSTEM AND METHOD FOR ACTIVE CONTROL OF ETCH PROCESS

**Mail Stop Appeal Brief - Patents**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

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## APPEAL BRIEF

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Dear Sir:

Applicants submit this Appeal Brief in triplicate in connection with an appeal of the above-identified patent application. Please charge $330.00 for the fee associated with this brief to Deposit Account No. 50-1063 [AMDP662US].

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## I. Real Party in Interest (37 C.F.R. §1.192(c)(1))

The real party in interest in the present appeal is American Micro Devices, Inc., the assignee of the present application.

## II. Related Appeals and Interferences (37 C.F.R. §1.192(c)(2))

Appellants, appellants' legal representatives, and/or the assignee of the present application are not aware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. Status of Claims (37 C.F.R. §1.192(c)(3))

Claims 1-12 and 25 are currently pending in the subject application and are presently under consideration. The rejection of claims 1-9 and 25 is appealed.

## IV. Status of Amendments (37 C.F.R. §1.192(c)(4))

No claim amendments have been entered subsequent the Final Office Action.

## V. Summary of Invention (37 C.F.R. §1.192(c)(5))

The subject invention generally relates to monitoring and controlling an etch process by utilizing real-time feed forward control based upon scatterometry analysis. (*See* pg. 1, ln. 5-7). The invention as claimed employs a light source that directs light onto one or more features of semiconductor wafer, and a light-capturing device to capture light reflected/refracted from the one or more features. (*See* pg. 3, ln. 13-17, pg. 8, ln. 5-12). For example, the features can be gratings, and light reflected from such gratings can be utilized to control an etching parameter (*See* pg. 3, ln. 15-17, pg. 10, ln. 1-5, p. 13, ln. 1-3). More particularly, scatterometry techniques can be employed, wherein light reflected from features upon a wafer (*e.g.,* gratings) generates a signature indicative of one or more etching parameters. (*See* pg. 3, ln. 18-23). This generated signature can thereafter be compared to stored signatures to facilitate proper adjustment of an etching process. (*See* pg. 3, ln. 29-32). Furthermore, the present invention provides a system and/or methodology that facilitates control of an etching process in an isolated area upon a wafer. (*See* pg. 4, ln. 25-33, pg. 17 ln. 3-6). Specifically, a wafer can be partitioned into grid blocks to facilitate determining positions or locations where a wafer may benefit from adjusting one or

more etch processes. *See* pg. 17, ln. 3-6). After partitioning, light can be directed onto a particular grid block, and the reflected light can be employed to generate a signature indicative of one or more etching parameters. (*See* pg. 17, ln. 21-23).

## VI. Statement of the Issues (37 C.F.R. §1.192(c)(6))

Whether claim 1 is unpatentable under 35 U.S.C. §103(a) as being obvious over Eriguchi, *et al.* (U.S. 6,113,733) in view of Su (U.S. 6, 486,492).

Whether claims 2-6 and 8 are unpatentable under 35 U.S.C. §103(a) over Eriguchi, *et al.* and Su in view of Xu, *et al.* (U.S. 6,483,580).

Whether claims 7 and 9 are unpatentable under 35 U.S.C. §103(a) over Eriguchi, *et al.*, Su, and Xu, *et al.* in view of Ko, *et al.* (U.S. 6,117,791).

Whether claim 25 is unpatentable under 35 U.S.C. §103(a) over Jahns (U.S. 5,711,843) in view of Su and further in view of Xu.

## VII. Grouping of Claims (37 C.F.R. §1.192(c)(7))

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1-12 and 25 stand or fall together.

## VIII. Argument (37 C.F.R. §1.192(c)(8))

**Rejection of Claim 1 under 35 U.S.C. §103(a)**

Claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Eriguchi, *et al.* (U.S. 6,113,733) in view of Su (U.S. 6,486,492). Reconsideration and allowance of claim 1 is respectfully requested for at least the following reasons. The Examiner has not established a *prima facie* case of obviousness as required by M.P.E.P. 706.02(j), which states:

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed

> combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner has not established a *prima facie* case of obviousness as required *supra*. No motivation to modify the reference exists, no reasonable expectation of success exists and not all of the claim limitations are taught or suggested by the reference. For these reasons and the reasoning *infra*, this rejection should be withdrawn.

In particular, and as will be discussed in detail below, neither Eriguchi, *et al.* nor Su teach or suggest ***directing... light onto one or more gratings located on at least one portion of the wafer*** and ***measuring one or more etching parameters from light reflected from the one or more gratings*** as recited in claim 1. The present invention as recited in this claim directs light upon ***one or more gratings***, and thereafter utilizes the reflected light to ***measure one or more etching parameters***. The light reflected from the ***one or more gratings*** is captured and employed to determine various parameters related to an etching process, including but not limited to size of features on a wafer, shape of features on a wafer, location of features on a wafer, chemical properties of a wafer, size of gratings, shape of gratings, location of gratings, size of space between features, shape of space between features, and location of space between features. Thus the present invention as recited in this claim can be employed to measure various critical dimensions related to at least a portion of a wafer directly *via* ***directing... light onto one or more gratings...*** and ***measuring one or more etching parameters from light reflected from the one or more gratings***. Furthermore, the present invention as claimed ***analyzes the etching parameter data by comparing the etching parameter data to stored etching data to generate a feed-forward control data operative to control the at least one etching component***. The present invention can thus be employed to control features measured *via* light reflected from ***the one or more gratings.*** Specifically, size of features, shape of features, dimensions of space between features, *etc.* can be measured and controlled *via* the present invention as claimed.

As stated above, Eriguchi, *et al.* does not disclose, teach, or suggest directing light towards ***one or more gratings...*** and ***measuring one or more etching parameters from light reflected from the one or more gratings.*** Specifically, Eriguchi, *et al. never* mentions "gratings" or light directed towards gratings. Rather, Eriguchi, *et al.* teaches a system for detecting defects in a semi-conductor region *via* emitting two light beams - an exciting light and a monitoring

light. The exciting light is utilized to excite carriers in the semiconductor region, thereby generating an electric field. The measuring light is directed at the same semiconductor region and reflects from the semiconductor region to a capturing mechanism. The reflectance of the monitoring light alters in the presence and absence of the exciting light. Therefore, the exciting light is intermittently emitted, and measurements of reflectance of the monitoring light are taken during instances the exciting light is applied as well as when the exciting light is not applied. A "change rate" is thereafter calculated based upon alteration in reflectance of the monitoring light in the presence and absence of the exciting light (*See* col. 6, lines 8-36). Such alteration of reflectance can thereafter be utilized to determine number of defects in the semiconductor region, thickness of film in the semiconductor region, and depth of damaged layers in the semiconductor region. Again, *nowhere* in Eriguchi, *et al.* is there mention of ***directing... light onto one or more gratings*** as recited in independent claim 1. Furthermore, Eriguchi, *et al.* cannot perform the type of control that is possible when employing the present invention as claimed. For example, the present invention as claimed can control size, shape, and location of features as well as size, shape, and location of spaces between such features *via* ***directing... light onto one or more gratings***. In contrast, Eriguchi, *et al.* utilizes the "change rate" to estimate number of defects in the semiconductor region, thickness of film in the semiconductor region, and depth of damaged layers in the semiconductor region. Eriguchi, *et al.* cannot measure size, shape, and location of features as well as size, shape, and location of spaces between such features, which can be accomplished by the present invention *via* ***directing... light onto one or more gratings***.

Su, like Eriguchi, *et al.*, does not disclose, teach, or suggest ***directing... light onto one or more gratings*** and ***measuring one or more etching parameters from light reflected from the one or more gratings.*** Rather, Su discloses a microscopy system utilized to monitor etching parameters, and then utilizing such monitored parameters as feed-forward information to facilitate control of a semiconductor manufacturing process. The microscopy techniques as taught in Su are expensive, time consuming, and can be destructive when compared to the optical system of the subject invention.

In view of at least the above, it is readily apparent that neither Eriguchi, *et al.* nor Su, alone or in combination, teach or suggest the subject invention as recited in independent claim 1. Accordingly, this rejection should be withdrawn.

**Rejection of Claims 2-6 and 8 under 35 U.S.C. §103(a)**

Claims 2-6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Eriguchi, *et al.* and Su, and further in view of Xu, *et al.* (U.S. 6,483,580). Withdrawal of this rejection is respectfully requested for at least the following reasons. Xu, *et al.* discloses a system for measuring film thickness and optical index of films underneath a diffracting structure utilizing a spectroscopic ellipsometer and an associated spectroscopic scatterometer. However, Xu, *et al.* does not disclose, teach, or suggest ***directing... light onto one or more gratings*** and ***measuring one or more etching parameters from light reflected from the one or more gratings***, and thus does not make up for the deficiencies of Eriguchi, *et al.* and Su. Therefore, this rejection should be withdrawn.

**Rejection of Claims 7 and 9 under 35 U.S.C. §103(a)**

Claims 7 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Eriguchi, *et al.*, Su, Xu, *et al.*, and further in view of Ko, *et al.* (U.S. 6,117,791). Withdrawal of this rejection is respectfully requested for at least the following reasons. Claims 7 and 9 depend from independent claim 1, and Ko, *et al.* does not make up for the aforementioned deficiencies of Eriguchi, *et al.* and Su. Therefore, the subject rejection should be withdrawn.

**Rejection of Claim 25 under 35 U.S.C. §103(a)**

Claim 25 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Jahns (U.S. 5,711,843) in view of Su and further in view of Xu. Reconsideration and allowance of this claim is respectfully requested for at least the following reasons. Neither Jahns, Su, nor Xu teaches or suggests combining all elements of the subject claim.

> Absent some teaching or suggestion in the prior art to combine elements, it is insufficient to establish obviousness by claiming that the separate elements of the invention existed in the prior art. *Arkie Lures Inc. v. Gene Larew Tackle Inc.*, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997).

Particularly, the cited references do not teach or suggest combining ***partitioning a wafer into... grid blocks*** and ***sensing the acceptability of etching in... grid blocks*** *via* ***scatterometry*** as recited in the subject claim. Jahns teaches monitoring process environment

properties, such as temperature of plasma, gas flow rate, gas pressure, *etc.* (*See* col. 3 lines 38-44). One or more of such sensed environmental properties are relayed to a process condition monitor, which determines whether any of such properties (or a combination of properties) renders the process defective. Utilizing the invention as disclosed in Jahns, an etching process is labeled as defective *based upon parameters within the process chamber*, and not based upon parameters of a wafer being processed. Furthermore, the system of Jahns cannot determine portions of a wafer that are defective. Rather, an entire wafer would be deemed defective (as defectiveness is determined based upon a process) even in an instance that only a small portion of such wafer was actually defective and could be repaired. Thus, Jahns does not teach or suggest means for controlling the etching of ***a wafer portion***, as it is not possible utilizing Jahns to ***sense the acceptability of etching in at least one of the one or more grid blocks*** as recited in the subject claim. Thus, utilizing Jahns, etching of an entire wafer can be controlled utilizing Jahns, but etching of ***a wafer portion*** cannot be controlled. Moreover, upon determining that environmental properties are such that etching the wafer is acceptable, etch rates (and various other process parameters) are *estimated* by a classifier based on the environmental properties. Such an arrangement does not facilitate control of etch components particular to grid cells of a wafer. Rather, the processes are controlled for the entire wafer, thus not facilitating achievement of critical dimensions throughout the entirety of the wafer.

Su teaches exposing a wafer to create a focus-exposure matrix, and thereafter examining each matrix cell with a conventional CD-SEM scan. Su does not teach or suggest utilizing ***scatterometry means*** for ***sensing the acceptability of etching in... grid blocks.*** As described above, CD-SEM scanning techniques as taught in Su are expensive, time consuming, and can be destructive when compared to the optical system of the subject invention. Xu discloses utilizing scatterometry techniques to measure one or more parameters of a diffracting structure. Xu does not teach or suggest utilizing scatterometry means for ***sensing acceptability of etching in a grid block*** of a wafer or ***partitioning a wafer into one or more grid blocks***.

The cited prior art references do not exhibit benefits obtained *via* utilizing the invention as recited in the subject claim to control an etching process on a portion of a wafer. Partitioning of the wafer into a grid enables accurate determination of a location in which control of an etching component is required. For example, *via* monitoring individual grid cells, an etching component can be controlled accordingly for those individual grid cells to facilitate achievement

of desirable critical dimensions throughout the wafer. Furthermore, the present invention enables *in situ* monitoring and control of an etching component pertaining to a particular grid cell without the expense, complexity, and risk associated with CD-SEM scans, which are known to be expensive, time consuming, and can be destructive. Moreover, etch rates and various other process parameters can be directly measured and controlled, rather than predicting such etch rates based upon processing environment properties such as temperature and gas flow as disclosed in Jahn. There is, however, no teaching or suggestion to utilize ***scatterometry means for sensing the acceptability of etching in at least one of the one or more grid blocks*** as recited in this claim. In general, the rationale proffered to combine such teachings is to achieve benefits identified in applicants' specification, to overcome problems associated with conventional methods, etc. Applicants' respectfully submit that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, the Examiner is basing the rejection on the assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in Applicants' specification. This sort of rationale has been condemned by the CAFC; see, for example, *Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987). More particularly, The Federal Circuit has consistently held that

> ...'***virtually all [inventions] are combinations of old elements.***' Therefore an examiner may often find every element of a claimed invention in the prior art. ***If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue.*** Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. ***Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'*** *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453 (Fed. Cir. 1998) (*citations omitted*).

The Examiner has also indicated that ***means for partitioning a wafer into one or more grid blocks*** can be interpreted as an entire front surface of a wafer. Applicants' representative respectively disagrees with this rationale. The term "partitioning" is defined as "The act or process of dividing something into parts" by The Fourth Edition of The American Heritage Dictionary. Thus, commensurate with the claim, the wafer has to be ***partitioned***, and a grid

block thus cannot be the entire wafer. It is possible, however, to ***partition*** a wafer so that it includes a single grid block (*e.g.*, a single square within the wafer). Therefore, as described *supra,* a particular portion of a wafer can be monitored, corrected, or deemed defective without requiring an entire wafer to be defective. Furthermore, Fig. 7 and accompanying text clearly illustrate that a grid block should not be interpreted as an entire front portion of a wafer.

> ***The specification acts as a dictionary when it expressly defines terms used in the claims*** or when it defines terms by implication. Where the patentee has clearly defined a claim term, that definition usually is dispositive; it is the single best guide to the meaning of a disputed term. *Guttman, Inc. v. Kopykake Enters.*, 302 F.3d 1352 (Fed. Cir. 2002) (citations omitted) (emphasis added).

Fig. 7 clearly shows that a grid block is not an entirety of a wafer, but that if desired a wafer could include a single grid block. The common definition of "partitioning" together with illustrations given in Fig. 7 make it abundantly clear that a grid block cannot be interpreted as an entire front surface of a wafer.

In view of the foregoing, it is respectfully submitted that no teaching or suggestion to combine Jahn, Su, and Xu exists in the cited references. Accordingly, this rejection should be withdrawn.

## IX. Conclusion

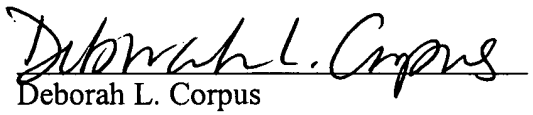
The present application is believed to be in condition for allowance, in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

AMIN & TUROCY, LLP



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## X. Appendix of Claims (37 C.F.R. § 1.192(c)(9))

1. (Previously Presented) A system for monitoring and regulating an etch process, comprising:

at least one etching component operative to etch at least one portion of a wafer;

an etch component driving system for driving the at least one etching component;

a system for directing a single beam of light onto one or more gratings located on at least one portion of the wafer;

an etch monitoring system operable to measure one or more etching parameters from light reflected from the one or more gratings; and

a processor operatively coupled to the etch monitoring system and the etch component driving system, wherein the processor receives an etching parameter data from the measuring system and analyzes the etching parameter data by comparing the etching parameter data to stored etching data to generate a feed-forward control data operative to control the at least one etching component.

2. (Original) The system of claim 1, the etch monitoring system further including a scatterometry system for processing the light reflected from the one or more gratings.

3. (Original) The system of claim 2, the processor being operatively coupled to the scatterometry system, the processor analyzing data received from the scatterometry system and producing an analyzed data and the processor controlling, at least in part, the at least one etching component *via* the etching component driving system based, at least in part, on the analyzed data.

4. (Previously Presented) The system of claim 3, wherein the etch process is at least one of descum etching, photoresist trim etching, breakthrough anti-reflective coating etching and main etching.

5. (Original) The system of claim 3, wherein the etch process is at least one of an isotropic etch process and an anisotropic etch process.

6. (Original) The system of claim 3, wherein the etch process is a dry-etching process where the mechanism of etching has at least one of a physical basis, a chemical basis and a combination of physical and chemical bases.

7. (Original) The system of claim 6, wherein the dry-etching technique with a mechanism of etching as a physical basis is at least one of a glow-discharge sputtering technique and an ion-milling technique.

8. (Original) The system of claim 6, wherein the dry-etching technique with a mechanism of etching as a chemical basis is a plasma etching technique.

9. (Original) The system of claim 8, wherein the dry-etching technique with a combination of bases is at least one of a reactive ion etching (RIE) technique and an ion-enhanced etching technique.

10. (Original) The system of claim 2, the processor logically mapping the wafer into one or more grid blocks and making a determination of the acceptability of etching values in the one or more grid blocks.

11. (Original) The system of claim 10, wherein the processor determines the existence of unacceptable etching values for at least a portion of the wafer based on comparing one or more measured etching values to one or more stored etching values.

12. (Original) The system of claim 11, wherein the processor employs a non-linear training system in computing feed-forward control data operable to adjust the at least one etching component.

13. (Withdrawn) A method for monitoring and regulating an etch process comprising:
logically partitioning a wafer into one or more portions;
fabricating one or more gratings to be etched on the wafer;

directing an incident light onto at least one of the one or more gratings;

collecting a reflected light reflected from the at least one grating;

measuring the reflected light to determine one or more critical dimensions associated with the at least one grating;

computing one or more adjustments for one or more etching components by comparing the one or more critical dimensions to scatterometry signatures associated with one or more stored critical dimensions; and

adjusting the etch process based, at least in part, on the one or more adjustments.

14. (Withdrawn) The method of claim 13, further comprising processing the reflected light in a scatterometry system.

15. (Withdrawn) The method of claim 14 wherein computing the one or more adjustments is based, at least in part, on data received from the scatterometry system.

16. (Withdrawn) The method of claim 15, wherein the etch process is regulated for portions of the wafer that have been etched.

17. (Withdrawn) The method of claim 15 wherein the etch process is regulated for unetched portions on the wafer that have not been etched.

18. (Withdrawn) The method of claim 15, wherein the etch process is regulated for subsequent wafers.

19. (Withdrawn) The system of claim 15, wherein the etch process is a dry-etching process where the mechanism of etching has at least one of a physical basis, a chemical basis and a combination of physical and chemical bases.

20. (Withdrawn) The system of claim 19, wherein the dry-etching technique with a mechanism of etching as a physical basis is at least one of a glow-discharge sputtering technique and an ion-milling technique.

21. (Withdrawn) The system of claim 19, wherein the dry-etching technique with a mechanism of etching as a chemical basis is a plasma etching technique.

22. (Withdrawn) The system of claim 19, wherein the dry-etching technique with a combination of bases is at least one of a reactive ion etching (RIE) technique and an ion-enhanced etching technique.

23. (Withdrawn) A method for monitoring and regulating an etch process comprising:

logically partitioning a wafer into one or more grid blocks;

etching the wafer with one or more etching components, where the one or more etching components are operable to etch at least one of the one or more grid blocks;

directing an incident light on at least one of the one or more grid blocks;

monitoring the etch process in at least one of the one or more grid blocks by analyzing light reflected from the at least one of the one or more grid blocks; and

coordinating control of at least one of the one or more etching components based, at least in part, on the analysis of the light reflected from the at least one of the one or more grid blocks.

24. (Withdrawn) The method of claim 23, wherein the one or more grid blocks are measured at pre-determined intervals of time.

25. (Original) A system for monitoring and regulating an trim process, comprising:

means for partitioning a wafer into one or more grid blocks;

scatterometry means for sensing the acceptability of etching in at least one of the one or more grid blocks;

means for controlling the etching of a wafer portion; and

means for selectively controlling the means for etching.